



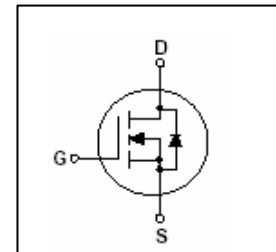
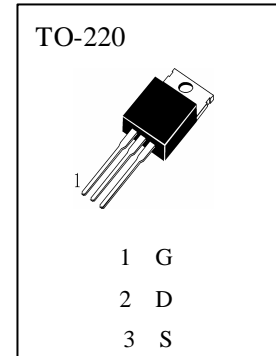
HFP4N60

APPLICATIONS

High-Speed Switching.

ABSOLUTE MAXIMUM RATINGS ($T_a=25$)

T_{stg}	—Storage Temperature.....	-55~150
T_j	—Operating Junction Temperature	150
P_D	— Allowable Power Dissipation($T_c=25$).....	100W
V_{DSS}	— Drain-Source Voltage	600V
V_{GSS}	— Gate-Source Voltage	$\pm 30V$
I_D	— Drain Current($T_c=25$).....	4.0A



ELECTRICAL CHARACTERISTICS ($T_a=25$)

Symbol	Characteristics	Min	Typ	Max	Unit	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	600			V	$I_D=250 \mu A, V_{GS}=0V$
I_{DSS}	Zero Gate Voltage Drain Current			10	μA	$V_{DS}=600V, V_{GS}=0$
I_{GSS}	Gate -Source Leakage Current			± 100	nA	$V_{GS}=\pm 30V, V_{DS}=0V$
$V_{GS(th)}$	Gate Threshold Voltage	2.0		4.0	V	$V_{DS}=V_{GS}, I_D=250 \mu A$
$R_{DS(on)}$	Static Drain-Source On-Resistance		2.0	2.5	Ω	$V_{GS}=10V, I_D=2.0A$
C_{iss}	Input Capacitance		710	920	pF	$V_{DS}=25V, V_{GS}=0, f=1MHz$
C_{oss}	Output Capacitance		65	85	pF	
C_{rss}	Reverse Transfer Capacitance		14	19	pF	
$t_{d(on)}$	Turn - On Delay Time		20	50	nS	$V_{DD}=300V, I_D=4.0A$ $R_G=25 \Omega$ *
t_r	Rise Time		55	120	nS	
$t_{d(off)}$	Turn - Off Delay Time		70	150	nS	
t_f	Fall Time		55	120	nS	$V_{DS}=480V$ $V_{GS}=10V$ $I_D=4.0A$ *
Q_g	Total Gate Charge		22	29	nC	
Q_{gs}	Gate-Source Charge		4.8		nC	
Q_{gd}	Gate-Drain Charge		8.5		nC	
I_S	Continuous Source Current			4.0	A	
V_{SD}	Diode Forward Voltage			1.5	V	$I_S=4.0A, V_{GS}=0$
$R_{th(j-c)}$	Thermal Resistance , Junction-to-Case			1.25	/W	

*Pulse Test : Pulse Width 300 μs , Duty Cycle 2%

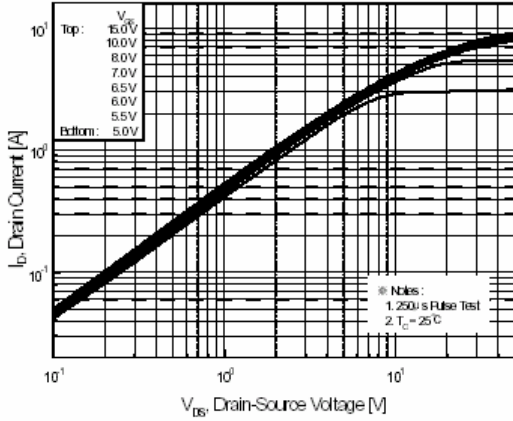


Figure 1. On-Region Characteristics

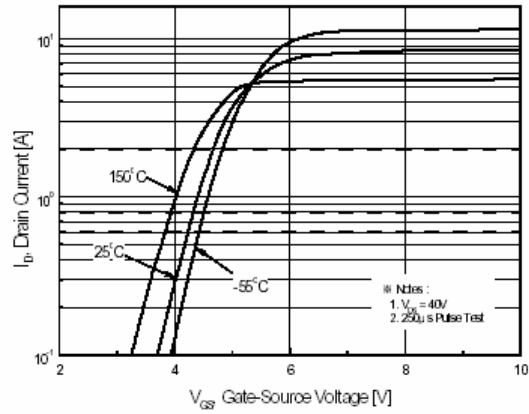


Figure 2. Transfer Characteristics

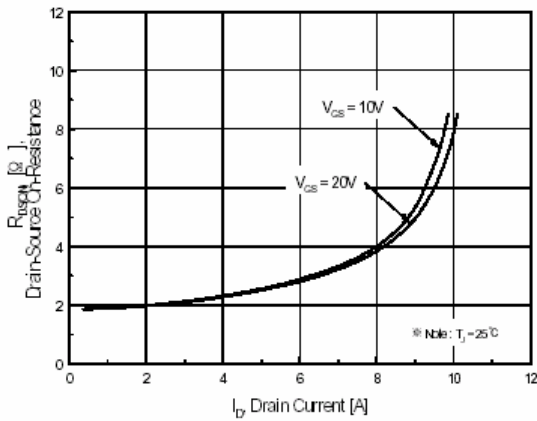


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

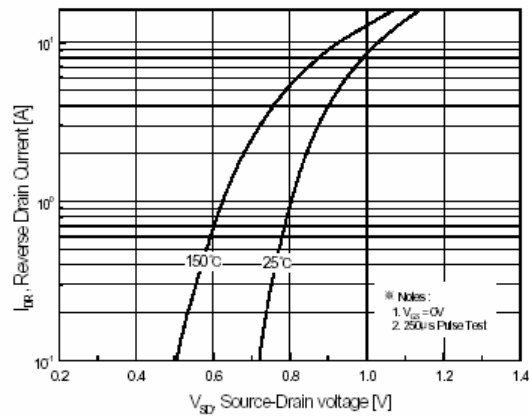


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

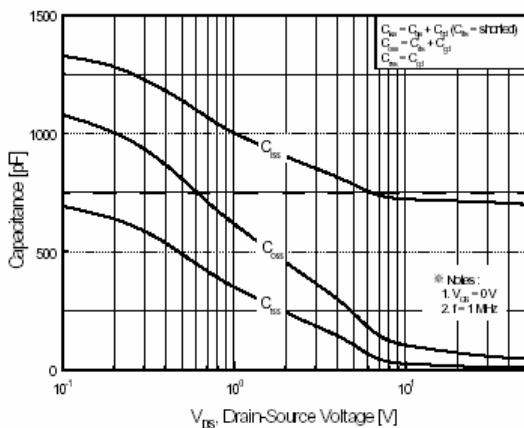


Figure 5. Capacitance Characteristics

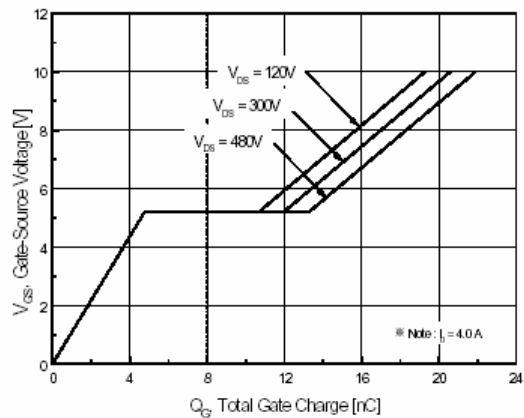


Figure 6. Gate Charge Characteristics



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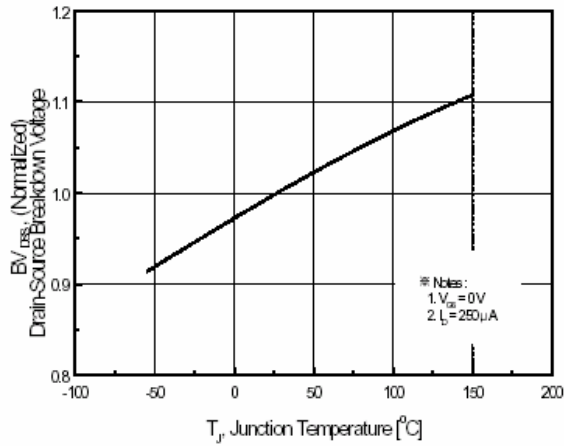


Figure 7. Breakdown Voltage Variation vs Temperature

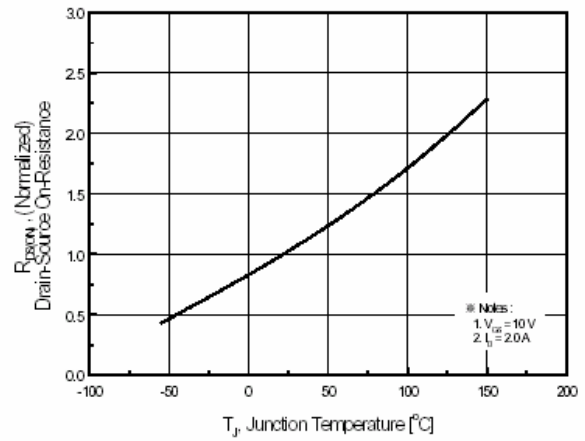


Figure 8. On-Resistance Variation

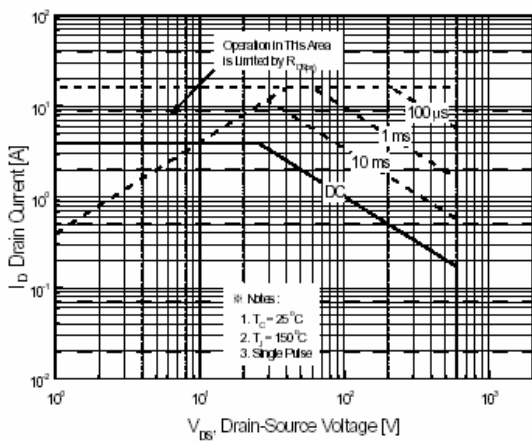


Figure 9-1. Maximum Safe Operating Area for HFP4N60

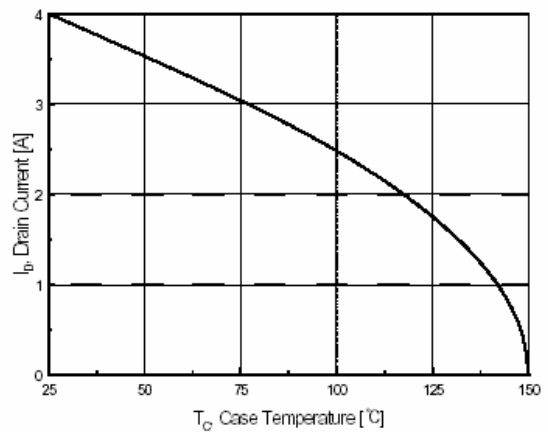


Figure 10. Maximum Drain Current vs Case Temperature

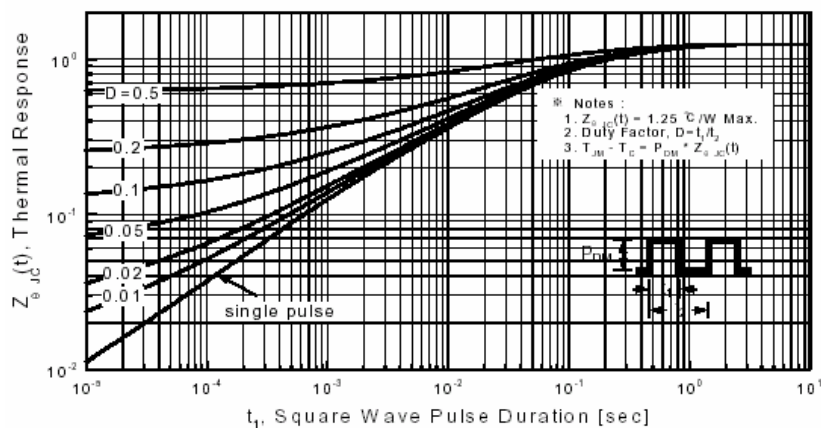
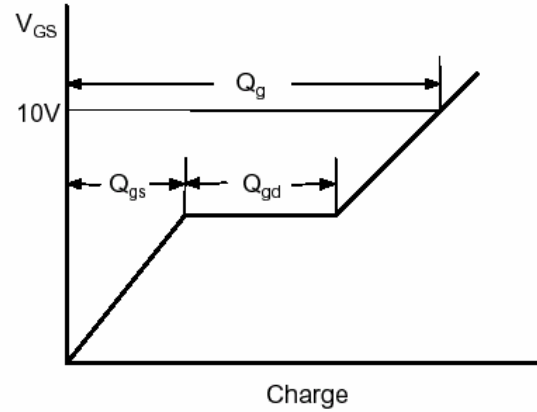
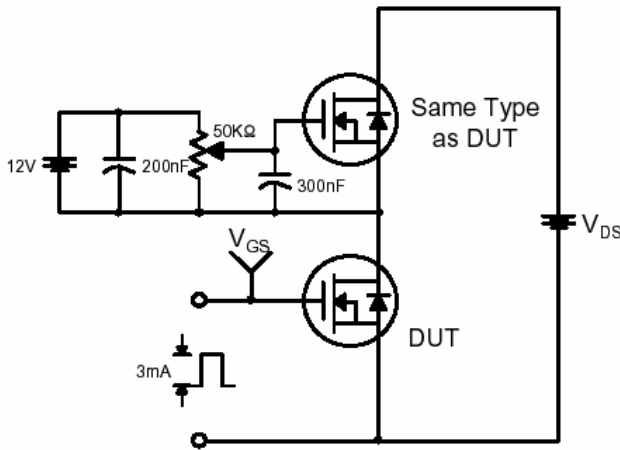


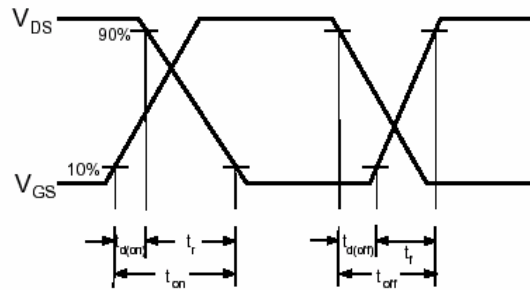
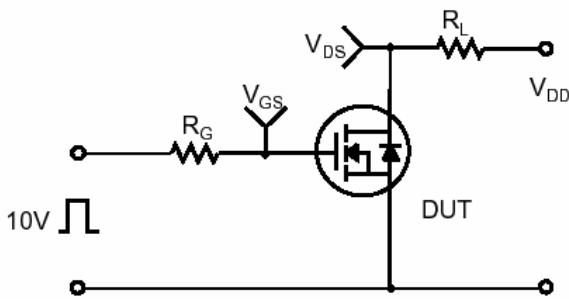
Figure 11-1. Transient Thermal Response Curve for HFP4N60



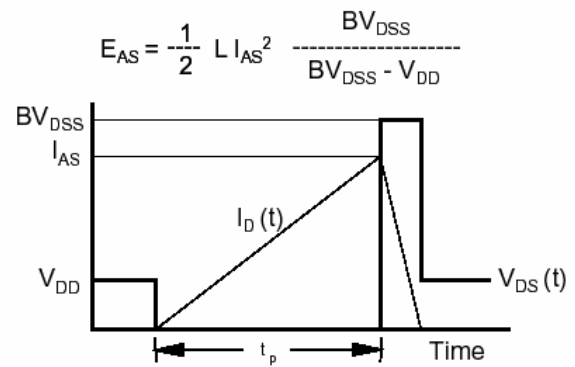
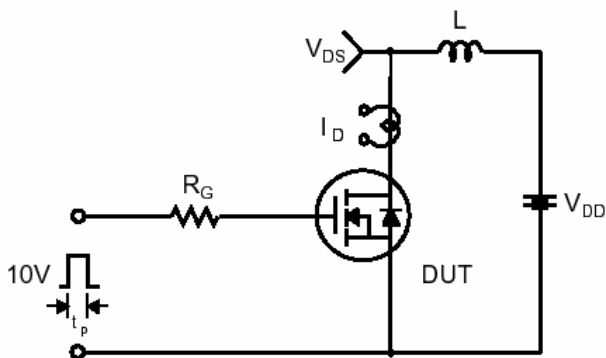
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



Peak Diode Recovery dv/dt Test Circuit & Waveforms

